

**North South University**

Department of Electrical & Computer Engineering

**ASSIGNMENT**

Course Name: Digital Logic Design  
Course Code: CSE231  
Section: 01

Assignment Number: 01

|  |
| --- |
| Assignment Name: Construct the necessary truth table(s), Boolean functions and Simulation file with the appropriate IC diagram comprising the basic logic gates that represent the given scenario. |

Submitted To: Taoseef Ishtiak

Assignment Date: August 16, 2020 Submission Date: August 16, 2020

Section: 01 Group Numbers: 15

|  |  |  |
| --- | --- | --- |
| Student Name: | Student ID: | Score |
| Md. Saron Ahmed | 1821641642 |
|  |  |
|  |  |
|  |  |
| Remarks: | |

**Experiment: 01**

**Concept:**

1.Understand the concept of binary addition and subtraction.

2. learn about half and full binary adders.

3.Performe binary addition and subtraction by using IC74283 adders.

4. Understand the concept of BCD addition and implements a BCD adder.

**Instrument:**

• Trainer Board

• 1 x IC 74283 4-bit binary adder

• 2 x IC 7486 quadruple 2-input XOR gate

* Wires

**Experiment 1:**

Table F.1.1

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Operation | M | A | B | C out | S4 S3 S2 S1 |
| 7+5 | 0 | 0111 | 0101 | 0 | 1100 |
| 4+6 | 0 | 0100 | 0110 | 0 | 1010 |
| 9+11 | 0 | 1001 | 1011 | 1 | 0100 |
| 15+15 | 0 | 1111 | 1111 | 1 | 1110 |
| 7-5 | 1 | 0111 | 0101 | 1 | 0010 |
| 4-6 | 1 | 0100 | 0110 | 0 | 1110 |
| 11-2 | 1 | 1011 | 0010 | 1 | 1001 |
| 15-15 | 1 | 1111 | 1111 | 1 | 0000 |

**Experiment: 02**

**Concept:**

BCD Adder

**Instrument:**

• Trainer board

• 2 x IC 74283 4-bit binary adder

• 1 x IC 7408 quadruple 2-Input AND gates

• 1 x IC 7432 quadruple 2-Input OR gates

F.2 Experimental Data (BCD Adder):

Table F.2.1

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| C out | Z3 | Z2 | Z1 | Z0 | C | S3 | S2 | S1 | S0 | Decimal |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 2 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 3 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 4 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 5 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 6 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 7 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 8 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 9 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 10 |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 11 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 12 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 13 |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 14 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 15 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 16 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 17 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 18 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 19 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 20 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 21 |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 22 |
| 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 23 |

Table F.2.2

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Operation | A | B | Over flow carry | Sum |
| 9+0 | 1001 | 0000 | 0 | 1001 |
| 9+1 | 1001 | 0001 | 1 | 0000 |
| 9+2 | 1001 | 0010 | 1 | 0001 |
| 9+3 | 1001 | 0011 | 1 | 0010 |
| 9+4 | 1001 | 0100 | 1 | 0011 |
| 9+5 | 1001 | 0101 | 1 | 0100 |
| 9+6 | 1001 | 0110 | 1 | 0101 |
| 9+7 | 1001 | 0111 | 1 | 0110 |
| 9+8 | 1001 | 1000 | 1 | 0111 |
| 9+9 | 1001 | 1001 | 1 | 1000 |